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Image AF/2857

Our Docket No.: 0325.00418

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Applicant	Steven P. Larkey, et al.		
Application No.:	09/658,597	Examiner:	West, J.
Filed:	September 11, 2000	Art Group:	2857
For:	UNIVERSAL SERIAL BUS (USB) GOLDEN PRODUCTION TEST MODE		

I hereby certify that this letter, the response or amendment attached hereto are being deposited with the United States Postal Service as first class mail in an envelope addressed to Mail Stop Appeal Brief Patent, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on April 5, 2004.

By: _____
Chris Maiorana

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Appellants submit, in triplicate, the following Appeal Brief pursuant to 37 C.F.R. §1.192 for consideration by the Board of Patent Appeals and Interferences. Appellants also submit herewith a PTO-2038 Form in the amount of $330.00 to cover the cost of filing the opening brief as required by 37 C.F.R. §1.17(c). Please charge any additional fees or credit any overpayment to our Deposit Account Number 50-0541.

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I. REAL PARTY IN INTEREST

The real party in interest is the Assignee, Cypress Semiconductor Corporation.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known to the Appellants, Appellants' legal representative, or Assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-20 are pending and remain rejected. The Appellants hereby appeal the rejection of claims 1-20.

IV. STATUS OF AMENDMENTS

Appellants are appealing a final Office Action issued by the Examiner on November 4, 2003. On December 11, 2003, Appellants filed a response requesting reconsideration. On January 21, 2004, the Examiner issued an Advisory Action indicating that the request was considered and that the rejection was maintained. On February 3, 2004, Appellants filed a Notice of Appeal.

V. SUMMARY OF INVENTION

The present invention concerns an apparatus generally comprising a low speed tester (302) and a host emulator (306). The host emulator may have (i) a first interface (320) coupled to the low speed tester to receive a test vector (TA) at a first speed, (ii) a second interface (324) configured to

(a) transmit the test vector to a device (310) at a second speed faster than the first speed and (b) receive a response from the device and (iii) a third interface (322) to the low speed tester to transfer a signal (RE) based upon the response, wherein the apparatus is configured to allow the low speed tester to perform high speed tests of the device at the second speed.

VI. ISSUES

The issue is whether claims 1-20 are patentable under 35 U.S.C. §103(a) over "SBAE-10 Bus Analyzer-Exerciser User's Manual" by Catalyst Enterprises, Inc. (hereafter Catalyst 1) and "Analyzer/Exercise/Tester" specification sheet by Catalyst Enterprises, Inc. (hereafter Catalyst 2) in view of Goutzoulis et al., U.S. Patent No. 5,177,630 (hereafter Goutzoulis).

VII. GROUPING OF CLAIMS

Appellants contend that the claims of the present invention do not stand or fall together. In particular, the following groups of claims are separately patentable:

Group 1: Claims 1,2,4,5,6,7,8,9,10,16,18 and 19 stand together.

Group 2: Claim 15 stands alone.

Group 3: Claims 3 and 17 stand together.

Group 4: Claims 11 and 12 stand together.

Group 5: Claim 13 stands alone.

Group 6: Claims 14 and 20 stand together.

The claim(s) in each group is(are) separately patentable from the claim(s) in any other groups.

VIII. ARGUMENTS

A. 35 U.S.C. § 103

"[T]o establish obviousness based on a combination of the elements disclosed in the prior art, there must be some motivation, suggestion or teaching of the desirability of making the specific combination that was made by the applicants."[1] "[T]he factual inquiry whether to combine references must be thorough and searching."[2] "This factual question ... [cannot] be resolved on subjective belief and unknown authority."[3] "It must be based on objective evidence of record."[4] The Examiner must show that (a) there is some suggestion or motivation, either in the references or in the knowledge generally available to one of ordinary skill in the art, to modify or combine the references, (b) there is a reasonable expectation of success, and (c) the prior art reference (or combination of references) teaches or suggests all of the claim limitations as arranged in the claims.[5] Furthermore, The Court of Appeals for the Federal Circuit has indicated that the requirement for showing the teaching of motivation to combine references is "rigorous" and must be "clear and particular".[6]

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[1] *In re Kotzab*, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1316 (Fed. Cir. 2000) (citing *In re Dance*, 160 F.3d 1339, 1343, 48 USPQ2d 1635, 1637 (Fed. Cir. 1998); *In re Gordon*, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984)).

[2] *McGinley v. Franklin Sports, Inc.*, 262 F.3d 1339, 1351-52, 60 USPQ2d 1001, 1008 (Fed. Cir. 2001).

[3] *In re Lee*, 277 F.3d 1338, 1343-44, 61 USPQ2d 1430, 1434 (Fed. Cir. 2002).

[4] *Id.* at 1343, 61 USPQ2d at 1434.

[5] Manual of Patent Examining Procedure (M.P.E.P.), Eighth Edition, Revised February 2003, §2142.

[6] *In re Anita Dembiczak* and *Benson Zinbarg*, 50 U.S.P.Q.2d 1614 (Fed. Cir. 1999)

1. **Group 1 (claims 1,2,4,5,6,7,8,9,10,16,18 and 19) is fully patentable over Catalyst 1, Catalyst 2 and Goutzoulis**

The claims of group 1 provide a host emulator having (i) a first interface coupled to a low speed tester to receive a test vector at a first speed and (ii) a second interface configured to transmit the test vector to a device at a second speed faster than the first speed. The Examiner asserts that it would have been obvious to combine Goutzoulis with Catalyst 1 and Catalyst 2 to cause a first USB between a personal computer (PC) and a host SBAE-10 of Catalyst 1 and Catalyst 2 to operate at a first speed and a second USB between the host SBAE-10 and an exercised SBAE-10 of Catalyst 1 and Catalyst 2 to operate at a second speed faster than the first speed.[7] However, the Examiner fails to state if the proposed combination slows the first speed for the first USB and/or increases the second speed for the second USB.

Assuming, *arguendo*, that a first possible modification slows the first speed, no motivation appears to exist to modify Catalyst 1 and Catalyst 2. In particular, one of ordinary skill in the art would appear not to have any realistic motivation for modifying Catalyst 1 and Catalyst 2 to **intentionally decrease a performance** of the first USB between the PC and the host SBAE-10 relative to the second USB. Furthermore, both Catalyst 1 and Catalyst 2 appear to be silent regarding a reasonable FIFO capability in the host SBAE-10 to buffer data passing between the first USB and the second USB at different rates. The Examiner does not provided any evidence showing that an SBAE-10 can operate with the first USB running at a slower speed than the second USB. As such, one of ordinary skill in the art would appear to be motivated to operate the fist USB at the same speed as the second USB to avoid a data bottleneck in the host SBAE-10. Furthermore, the

[7] Office Action, November 4, 2003, page 3, line 16 thru page 4, line 3.

fact that references can be combined or modified is not sufficient to establish *prima facie* obviousness.[8] Therefore, no motivation appears to exist to slow the first USB and no reasonable expectation of success has been established for the first possible modification.

Assuming, *arguendo*, that a second possible modification increases the second speed, no reasonable expectation of success appears to exist. In particular, Goutzoulis appears to teach how to convert a parallel signal loaded in a memory 10 into a serial signal transferrable to a device under test (DUT) 28 at high-speed through variable optical time-delay devices 20 and 24.[9] Therefore, the proposed modified host SBAE-10 would appear to transfer data on the second USB at a speed that is (i) faster than the data was received via the first USB and thus (ii) faster than the USB 1.1 standard. In contrast, both Catalyst 1 and Catalyst 2 appear to be silent, and no evidence or argument exists to show that the host SBAE-10 can buffer data between the first USB and the second USB operating at different rates. As such, no reasonable expectation for success of the second possible modification has been established.

Furthermore, since the proposed modified host SBAE-10 transmits at high-speed, the exercised SBAE-10 should also be modified to receive at the high-speed. However, each of Catalyst 1, Catalyst 2 and Goutzoulis appear to be silent regarding how to modify the exercised SBAE-10 to receive the high-speed serial signal from Goutzoulis. In addition, the Examiner does not provided any explanation or evidence how to modify the exercised SBAE-10 to receive at the high-speed. Thus, the second possible modification does not appear to have a reasonable expectation of success because (i) an unmodified exercised SBAE-10 does not appear to be capable of receiving the high-

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[8] M.P.E.P., Eighth Edition, Revised February 2003, §1243.01.

[9] Goutzoulis, column 2, line 60 through column 2, line 21 and FIG. 1.

speed signal and (ii) no obvious modification is established for a high-speed reception capability of the exercised SBAE-10. As such, *prima facie* obviousness has not been established for the claimed invention. Therefore, Catalyst 1, Catalyst 2 and Goutzoulis, alone or in combination, do not appear to teach or suggest a host emulator having (i) a first interface coupled to a low speed tester to receive a test vector at a first speed and (ii) a second interface configured to transmit the test vector to a device at a second speed faster than the first speed as presently claimed.

The claims of group 1 further provide a host emulator having a second interface configured to (a) transmit a test vector to a device and (b) receive a response from the device. In contrast, Goutzoulis appears to teach that the conversion from a low-speed parallel signal to high-speed serial signal produces a unidirectional interface.[10] In particular, an optoelectronic converter 26 used by Goutzoulis to present the high-speed signal in electrical form to the DUT 28 does not appear to be capable of receiving an electronic signal back from the DUT 28. Instead, Goutzoulis illustrates an electro-optical converter 30 for transmitting output signals from the DUT 28 back to a tester along a path separate from the input data.[11] As such, incorporating Goutzoulis into Catalyst 1 and Catalyst 2 would appear to result in splitting the second USB into two distinct unidirectional busses that would not connect with the host SBAE-10 at a single interface. Therefore, Catalyst 1, Catalyst 2 and Goutzoulis, alone or in combination, do not appear to teach or suggest a host emulator having a second interface configured to (a) transmit a test vector to a device and (b) receive a response from the device as presently claimed.

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[10] Goutzoulis, column 3, lines 14-21 and FIG. 1.

[11] Goutzoulis, FIG. 1.

The claims of group 1 further provide a host emulator having (i) a first interface coupled to a low speed tester to receive a test vector and (iii) a third interface to the low speed tester to transfer a signal based upon a response from a device. In contrast, Catalyst 1 appears to disclose only a single interface between the host SBAE-10 and the PC.[12] Catalyst 2 appears to be silent regarding two interfaces between the host SBAE-10 and the PC. Goutzoulis does not appear to teach the missing interface. Therefore, Catalyst 1, Catalyst 2 and Goutzoulis, alone or in combination, do not appear to teach or suggest a host emulator having (i) a first interface coupled to a low speed tester to receive a test vector and (iii) a third interface to the low speed tester to transfer a signal based upon a response from a device as presently claimed.

The Examiner takes Official Notice that two separate interfaces and a single bidirectional interface are known functional equivalents. However, the Examiner does not provided objective reasoning to split the first USB of Catalyst 1 into two interfaces. Instead, the Examiner merely asserts that it would have been obvious to separate the first USB because doing so "involves only routine skill in the art".[13] In contrast, the M.P.E.P. §2143.01 states:

> [The] fact that the claimed invention is within the capabilities of one of ordinary skill in the art in not sufficient by itself to establish *prima facie* obviousness.

Therefore, the only reason to separate the first USB of Catalyst 1 appears to be for alignment of the proposed combination with the claims. As such, *prima facie* obviousness has not been established to have two interfaces between the host SBAE-10 and the PC.

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[12] Catalyst 1, page 5, Figure 2.

[13] Office Action, November 4, 2003, page 4, line 12.

The claims of group 1 further provide a low speed tester performing high speed tests of a device at a second speed. In contrast, Catalyst 1 and Catalyst 2 each appear to be silent regarding the PC of Catalyst 1 operating at a low speed relative to the high speed testing of the exercised SBAE-10. Furthermore, the Examiner does not provided any evidence or explanation why the PC of Catalyst 1 is low speed relative to the exercised SBAE-10. As such, the assertion that the PC of Catalyst 1 is similar to the claimed low speed tester appears to be merely a conclusory statement lacking any supporting evidence.[14] Therefore, Catalyst 1, Catalyst 2 and Goutzoulis, alone or in combination, do not appear to teach or suggest a low speed tester performing high speed tests of a device at a second speed as presently claimed.

The Examiner does not provided clear and particular motivation to combine Catalyst 1 and Catalyst 2 with Goutzoulis. The asserted motivation to include Goutzoulis is to:

> [Provide a] method for producing the **high speed vectors required by Catalyst** in a method that applies for very high speed devices, provides necessary tester interconnections, and allows precise control of required DUT input time delays (column 2, lines 25-30 and column 3, lines 8-13). (Emphasis added)[15]

However, no evidence is provided that (i) "high speed vectors" faster than the USB 1.1 standard are "required by Catalyst", (ii) the exercised SBAE-10 is a "very high speed device" or that (iii) the second USB must allow for "precise control of required DUT input time delays", meaning "picosecond-type accuracy" per Goutzoulis.[16] Therefore, the asserted motivation does not appear to be based on text from Catalyst 1, Catalyst 2, Goutzoulis or knowledge generally available to one

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[14] Office Action, November 4, 2003, page 2, section 2, lines 5-6.

[15] Office Action, November 4, 2003, page3, last line through page 4, line 3.

[16] Goutzoulis, Abstract, last line.

of ordinary skill in the art per M.P.E.P. §2142. As such, *prima facie* obviousness to combine Catalyst 1 and Catalyst 2 with Goutzoulis has not been established.

In summary, the Examiner does not shown that Catalyst 1, Catalyst 2 and Goutzoulis, alone or in combination, teach or suggest a host emulator having (i) a first interface to a low speed tester configured to receive a test vector at a first speed, (ii) and a second interface configured to transmit the test vector at a second speed faster than the first speed and receive a response and (iii) a third interface to the low speed tester to transfer a signal based upon a response from a device as presently claimed. The Examiner does not shown that Catalyst 1, Catalyst 2 and Goutzoulis, alone or in combination, teach or suggest a low speed tester as presently claimed. The Examiner has not established *prima facie* obviousness for lack of clear and particular motivation to (i) combine Catalyst 1, Catalyst 2 and Goutzoulis and (ii) modify Catalyst 1 to have both a first interface and a third interface as presently claimed. The Examiner has not established *prima facie* obviousness for lack of evidence or explanation for a reasonable expectation of success for the proposed modification. As such, the claims of group 1 are fully patentable over the cited references and Official Notice and the rejection should be reversed.

2. Group 2 (claim 15) is fully patentable over Catalyst 1, Catalyst 2 and Goutzoulis

The claim of group 2 provides (i) means for transferring a test vector at a first speed to a first interface and (ii) means for transmitting the test vector from a second interface to a device at a second speed faster than the first speed. The Examiner asserts that it would have been obvious to combine Goutzoulis with Catalyst 1 and Catalyst 2 to cause a first USB between a personal computer (PC) and a host SBAE-10 of Catalyst 1 and Catalyst 2 to operate at a first speed and a second USB

between the host SBAE-10 and an exercised SBAE-10 of Catalyst 1 and Catalyst 2 to operate at a second speed faster than the first speed.[17] However, the Examiner fails to state if the proposed combination slows the first speed for the first USB and/or increases the second speed for the second USB.

Assuming, *arguendo*, that a first possible modification slows the first speed, no motivation appears to exist to modify Catalyst 1 and Catalyst 2. In particular, one of ordinary skill in the art would appear not to have any realistic motivation for modifying Catalyst 1 and Catalyst 2 to **intentionally decrease a performance** of the first USB between the PC and the host SBAE-10 relative to the second USB. Furthermore, both Catalyst 1 and Catalyst 2 appear to be silent regarding a reasonable FIFO capability in the host SBAE-10 to buffer data passing between the first USB and the second USB at different rates. The Examiner does not provided any evidence showing that an SBAE-10 can operate with the first USB running at a slower speed than the second USB. As such, one of ordinary skill in the art would appear to be motivated to operate the fist USB at the same speed as the second USB to avoid a data bottleneck in the host SBAE-10. Furthermore, the fact that references can be combined or modified is not sufficient to establish *prima facie* obviousness.[18] Therefore, no motivation appears to exist to slow the first USB and no reasonable expectation of success has been established for the first possible modification.

Assuming, *arguendo*, that a second possible modification increases the second speed, no reasonable expectation of success appears to exist. In particular, Goutzoulis appears to teach how to convert a parallel signal loaded in a memory 10 into a serial signal transferrable to a device under

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[17] Office Action, November 4, 2003, page 3, line 16 thru page 4, line 3.

[18] M.P.E.P., Eighth Edition, Revised February 2003, §1243.01.

test (DUT) 28 at high-speed through variable optical time-delay devices 20 and 24.[19] Therefore, the proposed modified host SBAE-10 would appear to transfer data on the second USB at a speed that is (i) faster than the data was received via the first USB and thus (ii) faster than the USB 1.1 standard. In contrast, both Catalyst 1 and Catalyst 2 appear to be silent, and no evidence or argument exists to show that the host SBAE-10 can buffer data between the first USB and the second USB operating at different rates. As such, no reasonable expectation for success of the second possible modification has been established.

Furthermore, since the proposed modified host SBAE-10 transmits at high-speed, the exercised SBAE-10 should also be modified to receive at the high-speed. However, each of Catalyst 1, Catalyst 2 and Goutzoulis appear to be silent regarding how to modify the exercised SBAE-10 to receive the high-speed serial signal from Goutzoulis. In addition, the Examiner does not provided any explanation or evidence how to modify the exercised SBAE-10 to receive at the high-speed. Thus, the second possible modification does not appear to have a reasonable expectation of success because (i) an unmodified exercised SBAE-10 does not appear to be capable of receiving the high-speed signal and (ii) no obvious modification is established for a high-speed reception capability of the exercised SBAE-10. As such, *prima facie* obviousness has not been established for the claimed invention. Therefore, Catalyst 1, Catalyst 2 and Goutzoulis, alone or in combination, do not appear to teach or suggest (i) means for transferring a test vector at a first speed to a first interface and (ii) means for transmitting the test vector from a second interface to a device at a second speed faster than the first speed as presently claimed.

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[19] Goutzoulis, column 2, line 60 through column 2, line 21 and FIG. 1.

The claim of group 2 further provides (i) means for transmitting a test vector from a second interface to a device and (ii) means for receiving a response from the device at the second interface. In contrast, Goutzoulis appears to teach that the conversion from a low-speed parallel signal to high-speed serial signal produces a unidirectional interface.[20] In particular, an optoelectronic converter 26 used by Goutzoulis to present the high-speed signal in electrical form to the DUT 28 does not appear to be capable of receiving an electronic signal back from the DUT 28. Instead, Goutzoulis illustrates an electro-optical converter 30 for transmitting output signals from the DUT 28 back to a tester along a path separate from the input data.[21] As such, incorporating Goutzoulis into Catalyst 1 and Catalyst 2 would appear to result in splitting the second USB into two distinct unidirectional busses that would not connect with the host SBAE-10 at a single interface. Therefore, Catalyst 1, Catalyst 2 and Goutzoulis, alone or in combination, do not appear to teach or suggest (i) means for transmitting a test vector from a second interface to a device and (ii) means for receiving a response from the device at the second interface as presently claimed.

The claim of group 2 further provides (i) means for transferring a test vector at a first speed to a first interface and (ii) means for transferring a signal based upon a response from a third interface. In contrast, Catalyst 1 appears to disclose only a single interface between the host SBAE-10 and the PC.[22] Catalyst 2 appears to be silent regarding two interfaces between the host SBAE-10 and the PC. Goutzoulis does not appear to teach the missing interface. Therefore, Catalyst 1, Catalyst 2 and Goutzoulis, alone or in combination, do not appear to teach or suggest (i) means for

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[20] Goutzoulis, column 3, lines 14-21 and FIG. 1.

[21] Goutzoulis, FIG. 1.

[22] Catalyst 1, page 5, Figure 2.

transferring a test vector at a first speed to a first interface and (ii) means for transferring a signal based upon a response from a third interface as presently claimed.

The Examiner takes Official Notice that two separate interfaces and a single bidirectional interface are known functional equivalents. However, the Examiner does not provided objective reasoning to split the first USB from Catalyst 1 into two interfaces. Instead, the Examiner merely asserts that it would have been obvious to separate the first USB because doing so "involves only routine skill in the art".[23] In contrast, the M.P.E.P. §2143.01 states:

> [The] fact that the claimed invention is within the capabilities of one of ordinary skill in the art in not sufficient by itself to establish *prima facie* obviousness.

Therefore, the only reason to separate the first USB of Catalyst 1 appears to be for alignment of the proposed combination with the claims. As such, *prima facie* obviousness has not been established to have two interfaces between the host SBAE-10 and the PC.

The Examiner does not provided clear and particular motivation to combine Catalyst 1 and Catalyst 2 with Goutzoulis. The asserted motivation to include Goutzoulis is to:

> [Provide a] method for producing the **high speed vectors required by Catalyst** in a method that applies for very high speed devices, provides necessary tester interconnections, and allows precise control of required DUT input time delays (column 2, lines 25-30 and column 3, lines 8-13). (Emphasis added)[24]

However, no evidence is provided that (i) "high speed vectors" faster than the USB 1.1 standard are "required by Catalyst", (ii) the exercised SBAE-10 is a "very high speed device" or that (iii) the second USB must allow for "precise control of required DUT input time delays", meaning

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[23] Office Action, November 4, 2003, page 4, line 12.

[24] Office Action, November 4, 2003, page3, last line through page 4, line 3.

"picosecond-type accuracy" per Goutzoulis.[25] Therefore, the asserted motivation does not appear to be based on text from Catalyst 1, Catalyst 2, Goutzoulis or knowledge generally available to one of ordinary skill in the art per M.P.E.P. §2142. As such, *prima facie* obviousness to combine Catalyst 1 and Catalyst 2 with Goutzoulis has not been established.

In summary, the Examiner does not shown that Catalyst 1, Catalyst 2 and Goutzoulis, alone or in combination, teach or suggest (i) means for transferring a test vector at a first speed to a first interface (ii) means for transmitting the test vector from a second interface to a device at a second speed faster than the first speed, (iii) means for receiving a response at the second interface and (iv) means for transferring a signal based upon the response from a third interface as presently claimed. The Examiner has not established *prima facie* obviousness for lack of clear and particular motivation to (i) combine Catalyst 1, Catalyst 2 and Goutzoulis and (ii) modify Catalyst 1 to have both a first interface and a third interface as presently claimed. The Examiner has not established *prima facie* obviousness for lack of evidence or explanation for a reasonable expectation of success for the proposed modification. As such, the claim of group 2 is fully patentable over the cited references and Official Notice and the rejection should be reversed.

3. Group 3 (claims 3 and 17) is fully patentable over Catalyst 1, Catalyst 2 and Goutzoulis

The claims of group 3 depend from the claims of group 1 and thus contains all of the limitations of group 1. Consequently, the arguments presented above in support of the patentability of group 1 are incorporated hereunder in support of group 3.

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[25] Goutzoulis, Abstract, last line.

The claims of group 3 further provide that a device (being tested) comprises a Universal Serial Bus (USB) device. As argued above for group 1, no motivation appears to exist to slow the first USB between the PC and host SBAE-10 of Catalyst 1. If Catalyst 1 and Catalyst 2 are modified to increase the speed of the second USB, then both the host SBAE-10 and the exercised SBAE-10 would be communicating with each other outside the boundaries of the USB 1.1 specification. An exercised SBAE-10 modified to communicate at high-speed using "ultrashort picosecond-type pulses"[26] does not appear to be USB compliant. Furthermore, the Examiner does not explain how the host SBAE-10 and the exercised SBAE-10 can communicate with each other outside the USB 1.1 standard and still be USB compliant. Therefore, Catalyst1, Catalyst 2 and Goutzoulis, alone or in combination, do not appear to teach or suggest a device comprising a Universal Serial Bus device as presently claimed. As such, the group 3 claims are fully patentable over the cited references and the rejection should be reversed.

4. Group 4 (claims 11 and 12) is fully patentable over Catalyst 1, Catalyst 2 and Goutzoulis

The claims of group 4 depend from the claims of group 1 and thus contains all of the limitations of group 1. Consequently, the arguments presented above in support of the patentability of group 1 are incorporated hereunder in support of group 4.

The claims of group 4 provide a device (under test) configured to transmit one or more test packets. In contrast, Catalyst 1, Catalyst 2 and Goutzoulis each appear to be silent regarding the exercised SBAE-10 and/or device under test being configured to transmit test packets. Furthermore,

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[26] Goutzoulis, column 2, lines 28-29.

the Examiner does not explain or provide any evidence how Catalyst 1, Catalyst 2 and/or Goutzoulis teach or suggest the exercised SBAE-10 and/or device under test generating a test packet.[27] Therefore, Catalyst 1, Catalyst 2 and Goutzoulis, alone or in combination, do not appear to teach or suggest a device configured to transmit one or more test packets as presently claimed. As such, the claims of group 4 are fully patentable over the cited references and the rejection should be reversed.

5. Group 5 (claim 13) is fully patentable over Catalyst 1, Catalyst 2 and Goutzoulis

The claim of group 5 depends from the claims of group 1 and thus contains all of the limitations of group 1. Consequently, the arguments presented above in support of the patentability of group 1 are incorporated hereunder in support of group 5.

The claim of group 5 further provides a low speed tester configured to generate a pass/fail signal. In contrast, the Examiner asserts that page 2 of Catalyst 1 and page 1, column 1 of Catalyst 2 provides a pass/fail signal similar to the claimed pass/fail signal.[28] The cited text of Catalyst 1 discussing signals appears to be:

> Inrush Current measurement (C10)
> This option allows you to measure inrush current over the first 10 milliseconds of device activation and displays a pass/fail result with respect to the USB compliance specifications.[29]

However, the Examiner asserts that the host SBAE-10 of Catalyst 1 is similar to the claimed **host**

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[27] Office Action, November 4, 2003, page 2, section 2 through page 4.

[28] Office Action, November 4, 2003, page 5, lines 12-14.

[29] Catalyst 1, page 2, last paragraph.

emulator.[30] Therefore, Catalyst 1 does not appear to contemplate an element similar to the claimed **low speed tester** generating a pass/fail type signal.

Furthermore, the cited text of Catalyst 2 states:

> Versatile
> SBAE-10 is a serial bus analyzer capable of analyzing and exercising data transfers for low and full speed protocols. The SBAE-10 is designed to be upgradeable to USB 2 so that the initial investment will be extended to the next generation.
>
> Host Software
> The SBAE-10 Software operates under Windows NT, 98 and 95.
>
> Testing USB HUB
> One upstream and one downstream auxiliary connectors allow for testing USB Hub input and output for testing the hub I/O ports.[31]

Nowhere in the above text, or in any other section does Catalyst 2 appear to discuss a pass/fail signal. Therefore, the assertion that Catalyst 2 teaches an element similar to the claimed low speed tester generating a pass/fail signal appears to be incorrect.

The Examiner further asserts that "Catalyst appears to provide test data to a user leaving the user to decide pass or fail".[32] However, a user of the PC of Catalyst 1 does not appear to be part of the PC (asserted to be similar to the claimed low speed tester). Furthermore, a decision made by a user does not appear to generate a signal. Therefore, the assertion by the Examiner that the user can decide pass or fail does not appear to establish that the PC of Catalyst 1 generates a pass/fail signal.

The Examiner further asserts that the pass/fail signal claim language is being "interpreted as

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[30] Office Action, November 4, 2003, page 2, section 2, lines 5-9.

[31] Catalyst 2, page 1, lower half of page, column 1.

[32] Office Action, November 4, 2003, page 5, lines 9-10.

test data that indicates whether the device passes or fails."[33] (Emphasis added). In contrast, M.P.E.P. §2111.01 states:

> When not defined by applicant in the specification, the words of a claim **must be given their plain meaning**. In other words, they must be read as they would have been **interpreted by those of ordinary skill in the art**. (Emphasis added)

The Examiner does not appear to be using the one-of-ordinary-skill-in-the-art standard in interpreting the pass/fail signal claim language. In particular, nowhere in the Office Actions or the Advisory does the Examiner show or explain how test data would be viewed by one of ordinary skill in the art as being similar to a pass/fail signal calculated from the test data and some pass/fail criteria. Furthermore, no explanation or rational is provided by the Examiner for expanding the phrase"pass/fail signal" beyond a plain and ordinary meaning for indicating a decision of either pass or fail. Therefore, the Examiner has failed to establish that Catalyst 1, Catalyst 2 and Goutzoulis, alone or in combination, teach or suggest a low speed tester configured to generate a pass/fail signal as presently claimed. As such, the claim of group 5 is fully patentable over the cited references and the rejection should be reversed.

6. Group 6 (claims 14 and 20) is fully patentable over Catalyst 1, Catalyst 2 and Goutzoulis

The claims of group 6 depends from the claims of group 1 and thus contains all of the limitations of group 1. Consequently, the arguments presented above in support of the patentability of group 1 are incorporated hereunder in support of group 6.

The claims of group 6 provide performing at least one test of a plurality of test modes

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[33] Office Action, November 4, 2003, page 5, lines 11-12.

wherein the plurality of test modes comprise USB 2.0 defined test modes for use in a production test environment. In contrast, Catalyst 1, Catalyst 2 and Goutzoulis each appear to be silent regarding USB 2.0 defined test modes. Furthermore, the assertion by the Examiner that "the invention of Catalyst discloses a plurality of test modes applicable in the USB 2.0 environment..." appears to be a conclusory statement.[34] No evidence or explanation is provided by the Examiner how Catalyst 1 and Catalyst 2 were able to allegedly disclose USB 2.0 defined test modes prior to the USB 2.0 specification being published. No cites into Catalyst 1, Catalyst 2 and/or Goutzoulis are provided by the Examiner pointing to actual USB 2.0 defined test modes. Catalyst 1 and Catalyst 2 merely appear to contemplate that the SBAE-10 is intended to be field upgradeable to some ambiguous future capability. Therefore, Catalyst 1, Catalyst 2 and Goutzoulis, alone or in combination, do not appear to teach or suggest performing at least one test of a plurality of test modes wherein the plurality of test modes comprise USB 2.0 defined test modes for use in a production test environment as presently claimed. As such, the claims of group 6 appear to be fully patentable over the cited references and the rejection should be reversed.

Groups 1-6 are separately patentable.

During prosecution, each independent and dependent claim is considered to be separately patentable over every other claim.[35] As such, each of the above groups is considered to be separately

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[34] Office Action, November 4, 2003, page 5, lines 20-22.

[35] See, e.g., *Rowe v. Dror*, 42 USPQ2d 1550, 1552 (Fed. Cir. 1997), *Preemption Devices, Inc. v. Minnesota Mining and Manufacturing Company*, 221 USPQ 841, 843 (Fed. Cir. 1984), and *Jones v. Hardy*, 727 F.2d 1524, 1528, 220 USPQ 1021, 1024 (Fed. Cir. 1984) (It is well established that each claim in a patent constitutes a separate invention.).

patentable over every other group.[36] In particular, each of the groups includes a unique combination of arguments that allow individual groups to stand over the references even if all of the other groups fall.

Group 1 includes an argument that Catalyst 1, Catalyst 2 and Goutzoulis do not teach or suggest a low speed tester as presently claimed. Since group 2 does not depend on the low speed tester argument, group 2 may be found patentable even if group 1 is not.

Group 3 includes an argument that Catalyst 1, Catalyst 2 and Goutzoulis do not teach or suggest a second interface between a host emulator and a device as presently claimed. Since groups 1-2 do not depend on the second interface argument, group 3 may be found patentable even if groups 1 and/or 2 are not.

Group 4 includes an argument that Catalyst 1, Catalyst 2 and Goutzoulis do not teach or suggest a device under test transmitting test packets as presently claimed. Since groups 1-3 do not depend on the device under test transmitting argument, group 4 may be found patentable even if groups 1-2 and/or 3 are not.

Group 5 includes an argument that Catalyst 1, Catalyst 2 and Goutzoulis do not teach or suggest generating a pass/fail signal as presently claimed. Since groups 1-4 do not depend on the pass/fail signal argument, group 5 may be found patentable even if groups 1-3 and/or 4 are not.

Group 6 includes an argument that Catalyst 1, Catalyst 2 and Goutzoulis do not teach or suggest USB 2.0 test modes as presently claimed. Since groups 1-5 do not depend on the USB 2.0 argument, group 6 may be found patentable even if groups 1-4 and/or 5 are not.

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[36] M.P.E.P., Eighth Edition, Revised February 2003, §1206.

B. CONCLUSION

None of the cited references, alone or in combination, appear to teach or suggest an apparatus and/or method for a low speed tester and a host emulator as presently claimed. Furthermore, the Examiner has failed to establish *prima facie* obviousness to combine the references. Hence, the Examiner has clearly erred with respect to the patentability of the claimed invention. It is respectfully requested that the Board overturn the Examiner's rejection of all pending claims, and hold that the claims are not rendered obvious by the cited reference. However, should the Board find the arguments herein in support of independent claims 1, 15, and/or 16 unpersuasive, the Board is respectfully requested to carefully consider the arguments set forth above in support of each of the independently patentable groups.

Respectfully submitted,

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IX. APPENDIX

The claims of the present application which are involved in this appeal are as follows:

1. An apparatus comprising:

a low speed tester; and

a host emulator having (i) a first interface coupled to said low speed tester to receive a test vector at a first speed, (ii) a second interface configured to (a) transmit said test vector to a device at a second speed faster than said first speed and (b) receive a response from said device and (iii) a third interface to said low speed tester to transfer a signal based upon said response, wherein said apparatus is configured to allow said low speed tester to perform high speed tests of said device at said second speed.

2. The apparatus according to claim 1, wherein said host emulator is further configured to perform a verification of said device.

3. The apparatus according to claim 1, wherein said device comprises a Universal Serial Bus (USB) device.

4. The apparatus according to claim 1, further comprising:

a test vector generator configured to transfer said test vector to said low speed tester.

5. The apparatus according to claim 4, wherein said low speed tester is configured to control said host emulator.

6. The apparatus according to claim 4, wherein said low speed tester is configured in response to said test vector.

7. The apparatus according to claim 6, wherein said test vector generator is configured to generate said test vector.

8. The apparatus according to claim 1, wherein said apparatus is further configured to test a reception and transmission operation of said device.

9. The apparatus according to claim 1, wherein said apparatus is further configured to initiate one or more test packets.

10. The apparatus according to claim 9, wherein said device is further configured to receive and verify said one or more test packets.

11. The apparatus according to claim 1, wherein said device is further configured to transmit one or more test packets.

12. The apparatus according to claim 11, wherein said host emulator is further configured to receive and verify said one or more test packets.

13. The apparatus according to claim 1, wherein said low speed tester is

further configured to generate a pass/fail signal.

14. The apparatus according to claim 1, wherein said apparatus is configured to perform at least one test of a plurality of test modes wherein said plurality of test modes comprise USB 2.0 defined test modes for use in a production test environment.

15. An apparatus comprising:

means for transferring a test vector at a first speed to a first interface;

means for transmitting said test vector from a second interface to a device at a second speed faster than said first speed;

means for receiving a response from said device at said second interface; and

means for transferring a signal based upon said response from a third interface to perform high speed tests of said device at said second speed.

16. A method for testing comprising the steps of:

(A) transferring a test vector at a first speed from a low speed tester to a first interface of a host emulator;

(B) transmitting said test vector from a second interface of said host emulator at a second speed faster than said first speed to a device;

(C) receiving a response from said device at said second interface; and

(D) transferring a signal from a third interface of said host emulator to said low speed tester based upon said response to perform high speed tests of said device at said second speed.

17. The method according to claim 16, wherein said device comprises a USB device.

18. The method according to claim 16, further comprising the step of:

configuring said low speed tester to control said host emulator.

19. The method according to claim 18, further comprising the step of:

generating said test vector external to said host emulator.

20. The method according to claim 16, further comprising performing at least one of a plurality of test modes wherein the plurality of test modes comprise USB 2.0 defined test modes for use in a production test environment.